

CMOS VOLTAGE BOOSTER CIRCUIT

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of copending commonly assigned U.S. Patent Application Serial Number 10/337,053 entitled CMOS
5 Voltage Booster Circuits filed January 6, 2003.

FIELD OF THE INVENTION

The present invention is generally related to voltage boosting circuits, and more particularly to pre-charging voltage boosting circuits.

BACKGROUND OF THE INVENTION

10 Figure 1 illustrates at 10 the concept of voltage boosting. The purpose of a voltage booster is to generate a specified voltage higher than VDD at node V-boosted, where VDD is the power supply voltage. A voltage booster basically contains two parts: a pre-charge circuit and a boosting capacitor (C boost). Before node Boost_Ctl is pulled to high, the pre-charge circuit charges node Ncb
15 to some positive voltage. Then, node Boost_Ctl is pulled to VDD and switch S1 is turned on to charge load capacitor C_load to a voltage level above VDD. This boosted voltage level is determined by the voltage at node Ncb before Boost_Ctl goes high and the ratio of C_boost/C_load. The lower the pre-charged voltage at node Ncb, the larger the capacitance ratio is needed, and the larger the area cost
20 for capacitor C_boost. Thus, it is best to pre-charge node Ncb to VDD before Boost_Ctl starts going high.

There are four ways known in the prior art of voltage boosters to pre-charge C_boost to VDD:

- 1) As shown in U.S. Patent 5,999,461 and 4,186,436, when the boosted voltage is needed, the pre-charge circuit is enabled, but Boost_Ctl is not pulled to high until node Ncb is charged to VDD. Obviously, the major disadvantage is that some delay must be introduced. Thus, this scheme is not applicable to high speed devices.
- 2) As shown in U.S. Patent 6,268,761 and 6,275,425, PMOS transistors are used to pre-charge node Ncb to VDD and keep the voltage at VDD during standby. The disadvantage is that the sizes of the PMOS transistors are huge when capacitor C_boost is large and pre-charging must be completed in a short time.
- 3) As shown in U.S. Patent 5,175,448 and 5,636,115, NMOS transistors with their gate boosted above VDD are used to pre-charge node Ncb to VDD during standby. The advantage of using NMOS transistors is that the sizes of the transistors can be much smaller due to the higher drive capability of NMOSFET than PMOSFET. However, the voltage at node Ncb cannot be kept at VDD for a long time due to various leakages. When the voltage at node Ncb decreases, the size of capacitor C_boost must be increased in order to boost the voltage to the same level.
- 4) As shown in U.S. Patent 5,701,096 charge pumps are used to continuously supply charge to capacitor C-boost and keep the voltage at some level. However, complex timing and control circuits must be introduced.

In one conventional memory application, a voltage booster is needed to boost the word line above VDD to $VDD + V_{thn}$, and the memory access time is about 11ns. This means that there is no time for pre-charging the boosting capacitor after the chip is enabled, and the cycle time is about 20ns. Thus, the

5 boost capacitor must be quickly pre-charged to VDD as soon as the memory access is terminated. In the technique described in 3) above, the NMOS transistors are used as pre-charge devices. The boost capacitor is huge (60pf) because the voltage on the booster capacitor decreases to a level below VDD due to the leakages. Furthermore, it takes a long time to pre-charge the boost

10 capacitor to VDD due to the huge size.

SUMMARY OF THE INVENTION

The embodiments of the present invention take the advantages of both PMOS and NMOS transistors. A NMOS transistor with its gate boosted above VDD to $VDD + V_{thn}$ is used to quickly charge the boosting capacitor to VDD at the end of each memory access and two small PMOS transistors connected back-to-back are used to keep the voltage at VDD during standby. This combination provides high speed with small devices and meets the voltage requirements. Compared the capacitor size is reduced from 60pf to 10pf, the power consumption is reduced by 76% during a memory access, and the boosting speed is significantly improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic depicting conventional voltage boosting;

Figure 2 is a schematic of one embodiment of the CMOS voltage booster according to the present invention;

5 Figure 3 is a graph of voltage VPWR with a 5pf load capacitor;

Figure 4 is a graph of various voltages illustrating that the voltage of node pg is the same potential as node VPWR during boosting;

Figure 5 is a graph exhibiting the voltages of VPWR and pg during two memory accesses;

10 Figure 6 is a graph of the voltage sequence for boosting the gate of NMOS transistor MN1;

Figure 7 is a schematic of a second embodiment of the CMOS voltage booster according to the present invention;

15 Figure 8 is a graph of VPWR with a 5pf load capacitor for the embodiment of Figure 6; and

Figure 9 is a graph of the voltage of node pg and node VPWR, where transistor MP3 effectively shorts nodes pg and VPWR, and turns transistor MP1 off during boosting.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to Figure 2 there is shown a detailed electrical schematic of a first preferred embodiment of the present invention being a CMOS voltage booster 20. This circuit 20 keeps the voltage of node VPWR at VDD when signal ENVPWR is low and boosts the voltage of node VPWR above VDD to $VDD + V_{thn}$ as soon as possible when signal ENVPWR becomes high, where VDD is the power source voltage and V_{thn} is the threshold voltage of a NMOS FET. Capacitor C1 is the main voltage booster capacitor which advantageously boosts the voltage at node VPWR when node inv2 becomes high. NMOS FET MN1 charges capacitor C1 to VDD and PMOS transistors MP1 and MP2 keep the VPWR voltage at VDD during standby.

An application of this circuit 20 is to boost the voltage at a word line of a memory device above VDD to $VDD + V_{thn}$ when signal ENVPWR is pulled to VDD and node VPWR is connected to the word line during a memory access.

Circuit 20 provides technical advantages by taking advantage of higher drive ability of a NMOS FET than a PMOS FET, whereby NMOSFET MN1 with its gate ng boosted above VDD to $VDD + V_{thn}$ is used to quickly charge the boosting capacitor C1 to VDD at the end of each memory access. However, the NMOSFET MN1 cannot keep the voltage at capacitor C1 at VDD for a long time and thus the voltage at VPWR will eventually decrease to a level below VDD due to various leakages. To overcome this, two small PMOS transistors MP1 and MP2 are advantageously provided to keep the voltage of node VPWR at VDD during standby. This combination takes both the advantages of NMOS and PMOS transistors to reach high speeds with small devices and also meet the voltage requirements over time.

Moreover, the gate of NMOSFET MN1 is boosted above VDD to $VDD + V_{thn}$ by a small capacitor C2 at the end of each memory access. The gate of NMOSFET MN2 is connected to node VPWR. When node VPWR is boosted above VDD to $VDD + V_{thn}$ during a memory access, the gate of NMOSFET MN2 is boosted to the same voltage and capacitor C2 is charged to VDD by NMOSFET MN2. Advantageously, no separate timing control and boosting circuits are needed for boosting the gate of NMOSFET MN2 with this design.

In addition, the gates of the PMOS transistors MP1 and MP2 are advantageously boosted by small capacitors C3 and C4 to a voltage close to the voltage at node VPWR to turn MP1 off when node VPWR is boosted above VDD by capacitor C1.

Advantageously, the moment that signal ENVPWR starts going high, node inv0 is still low. NMOSFET MN4 shunts node tell1 to low and NMOSFET MN3 charges capacitor C3 to some positive voltage. Similarly, NMOSFET MN4 charges node tell1 to some positive voltage when node inv2 is still low. Finally, when node inv2 becomes high, node VPWR and node pg are boosted above VDD at the same time. Thus, no separate timing control circuit is needed for boosting the gate of PMOS transistor MP1.

In addition, by simply tying the gates of NMOS transistors MN3 and MN4 to VDD, these two transistors are able to play two functions: discharge nodes pg and tell1 to ground when signal ENVPWR is low and isolate nodes pg and tell1 from nodes ENVPWR and inv0 when signal ENVPWR is high and nodes pg and tell are boosted above VDD.

Moreover, in this voltage booster circuit 20, the voltages at some nodes are boosted to a level higher than VDD and may cause some breakdown. Thus, the maximum gate voltage stress is an important reliability issue in any booster circuit. A big advantage for this circuit 20 is that the voltage applied between gate and source is always lower than VDD for all the transistors in the circuit 20. Thus, the maximum gate stress is always within the safe region.

Figure 3 graphically shows at 30 the voltage VPWR at node VPWR from spice simulation for a nominal process, room temperature and VDD = 1.3V, with a 5pf load capacitor connected to the VPWR. As shown at 32, when signal ENVPWR becomes high, node VPWR can be boosted above 2.1V. When signal ENVPWR becomes low at the end of an access, the voltage at node VPWR can be recovered to VDD within 3ns and kept at VDD.

As shown in Figure 4, when signal ENVPWR starts going high at 10ns, voltage Vpg at node pg starts going up. After a slight delay node tell starts going up. At about 10.4ns, node inv2 starts going up. At this moment, the voltage at node pg is about 0.7V. At about 11.1ns, node inv2 reaches VDD, and the voltages at VPWR and pg are boosted to above 2.1V and 1.9V, respectively.

Figure 5 shows the voltages at node VPWR and node pg during two memory accesses. The voltage difference between node VPWR and node pg is less than 0.2V, thus transistor MP1 is kept off during boosting. At the end of boosting, node pg is quickly discharged to ground and transistors MP1 and MP2 are fully turned on to help charging of node VPWR back to VDD.

The voltages shown in Figure 6 exhibit the sequence of boosting the gate of NMOS transistor MN1. When signal ENVPWR becomes high, node inv1 goes low after a slight delay. Node ng is pulled below VDD. Note that this dip only occurs during the first memory access. After that, the capacitor C2 will be
5 charged to VDD during each memory access. After a small delay, node inv2 goes high and boosts node VPWR above VDD to $VDD + V_{thn}$. Since the gate of NMOS transistor MN2 is connected to node VPWR, NMOS transistor MN2 is fully turned on and drives node ng to VDD. NMOS transistor MN1 is off and capacitor C2 is charged to VDD. When signal ENVPWR becomes low, node
10 inv1 goes high after a slight delay and capacitor C2 boosts the gate of NMOS transistor MN1 above VDD to $VDD + V_{thn}$. NMOS transistor MN1 is fully turned on and quickly drives node VPWR back to VDD.

Referring now to Figure 7, there is shown a second preferred embodiment of the present invention, which is similar to the first preferred embodiment shown
15 and described in reference to Figure 2, wherein like numerals refer to like elements.

In the circuit 40, the small boost capacitors C3 and C4 are not utilized, and a PMOS FET MP3 shorts the output line VPWR to low at the moment voltage ENVPWR starts going high and node INV1 is still low. Similarly, transistor MP3
20 allows output line VPWR to achieve a positive voltage when node INV2 is still low. When node INV2 becomes high, VPWR and node pg are boosted above VDD at the same time. Advantageously, no separate timing control circuit is needed for boosting the gate of transistor MP1. The gate of transistor MN3 is tied to high, such that transistor MN3 discharges node pg to ground when control
25 signal ENVPWR is low and isolates node INV1 from ENVPWR when ENVPWR is high and node pg is boosted above VDD.

Like the circuit 10 of the first embodiment, circuit 40 prevents breakdown of transistors when boosting some nodes, including node pg, above VDD. Thus, the maximum gate voltage stress in the boost circuit is controlled providing a reliable circuit. Advantageously, all the transistors in circuit 40 are configured
5 such that a voltage applied between the respective gate and source is always lower than VDD, and the maximum gate stress is always within the safe region.

Figure 8 is a graph of signal VPWR of circuit 40 with a 5 pf load capacitor.

Figure 9 is a graph of the voltage of node pg and node VPWR where
10 transistor MP3 effectively shorts nodes pg and VPWR, and turns transistor MP1 off during boost.

Figure 6 also represents the voltage sequence for boosting the gate of NMOS transistor MN1 of circuit 40.

Though the invention has been described with respect to a specific
15 preferred embodiment, many variations and modifications will become apparent to those skilled in the art upon reading the present application. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.